FRONTGRADE Gaisler

PRODUCT BRIEF

RELEASED SEPTEMBER 2023

DUAL-CORE LEON3FT MICROPROCESSOR

GR712RC

The GR712RC is a fault tolerant dual-core LEON3FT SPARC V8 processor, with advanced interface protocols, dedicated for high reliability rad-hard aerospace applications. The GR712RC is fabricated at Tower Semiconductors Ltd., using standard 180 nm CMOS technology.

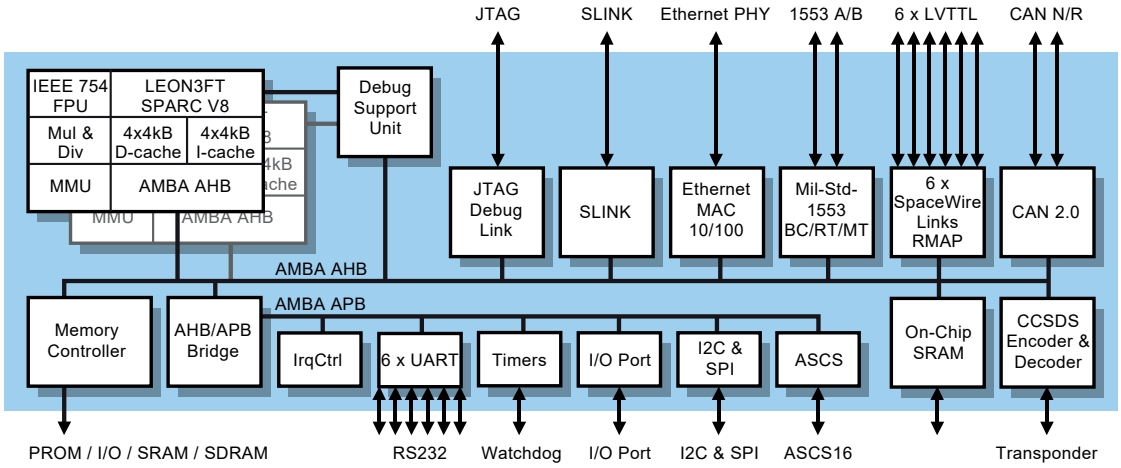
It employs radiation-hard-by-design methods from Gaisler and the RadSafeTM technology from Ramon Space Ltd., enabling superior radiation hardness together with excellent low-power performance.

The GR712RC provides a rich set of communication interfaces to allow different systems being implement using the same device type, which simplifies parts procurement. It also brings cost reductions to software development since the core functionality can be reused from application to application, only changing the drivers for the interfaces.

The GR712RC architecture is centred around the AMBA Advanced High-speed Bus (AHB), to which the two LEON3-FT processors and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB), which is accessed through an AHB to APB bridge.

The LEON3FT processors provide hardware support for cache coherency, processor enumeration and interrupt steering. Each processor core includes a SPARC Reference Memory Management Unit (SRMMU) and an IEEE-754 compliant double-precision FPU for floating point operations. It can be utilized in symmetric or asymmetric multiprocessing mode.

The LEON3FT embeds error detection and correction codes (ECC) in its internal memories enabling it to recover from radiation-induced soft errors. The ECC encoding/decoding is done in parallel with normal operation, and a correction cycle is fully transparent to the software, which can continue to run uninterrupted. Moreover, the external memory controller can optionally protect the PROM, SRAM and SDRAM areas with BCH ECC, allowing single-error correction and double-error detection for each 32-bit memory word. The SDRAM can also be protected by Reed Solomon coding, which can correct up to two 4-bit nibbles.



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Features:

- Two fault tolerant LEON3-FT SPARC V8 compliant 32-bit processors, each with:
  - SPARC reference memory management unit (SRMMU) with 32 TLB entries
  - High-performance double-precision IEEE-754 floating point co-processor (GRFPU)
  - 16 KiB multi-way instruction cache and 16 KiB multi-way data cache
- Instruction trace and AMBA (AHB) trace buffers for debugging
- Timer unit with four 32-bit timers including watchdog
- Secondary timer unit with four 32-bit timers
- Primary and secondary interrupt controller for 31 interrupts
- On-chip 192 kByte RAM memory block with EDAC
- External memory support:
  - Data bus width: 8 bits, or 32 bit data plus 8/16 bits for EDAC checkbits
  - 8 bit BCH EDAC for SRAM and PROM, 16 bit Reed-Solomon EDAC for SDRAM
  - Memory types: SRAM, SDRAM, FLASH, MRAM, EEPROM and parallel I/O
  - Programmable wait-states:
    - SRAM read/write cycle 2 - 5 clock cycles
    - PROM / EEPROM / NOR-FLASH read cycle 2 - 32 clock periods
- Debug Support Unit (DSU) accessed via JTAG and SpaceWire RMAP targets

Performance:

The two LEON3FT processor cores in the GR712RC can be clocked up to 100 MHz (depending on external device choices) over the full military temperature range. This provides up to 200 MIPS/200 MFLOPS peak performance. The typical core power consumption at room temperature is lower than 1 W.

Interfaces:

- Two dedicated SpaceWire ports with RMAP targets, maximum 200 Mbps full-duplex data rate
- Configurable I/O selection matrix, connecting available I/O units to 67 shared pins:
  - Four additional SpaceWire ports, maximum 200 Mbps full-duplex data rate
  - Redundant MIL-STD-1553B BRM (BC/RT/BM) interface
  - Two CAN 2.0B bus controllers
  - Six UART ports, with 8-byte FIFO
  - Ethernet MAC with RMII 10/100 Mbps port
  - SPI master serial port
  - I2C master serial port
  - ASCS16 (STR) serial port
  - SLINK 6 MHz serial port
  - CCSDS/ECSS 5-channel Telecommand decoder, 10 Mbps input rate
  - CCSDS/ECSS Telemetry encoder, 50 Mbps output rate
  - 26 input and 38 input/output general purpose ports

Software development:

The GR712RC development board for GR712RC is provided for prototyping and software development, together with development tools such as the TSIM instruction simulator and the GRMON software debugger, and various compilers and operating systems.

Packaging & quality:

The GR712RC can be delivered in three quality levels: flight, engineering and prototype.
It is provided in a 240-pin, 0.5 mm pitch hermetic ceramic quad flat package (CQFP-240).
Prototype devices and the GR712RC development board are available for immediate delivery.
GR712RC is not subject to U.S. export regulation.